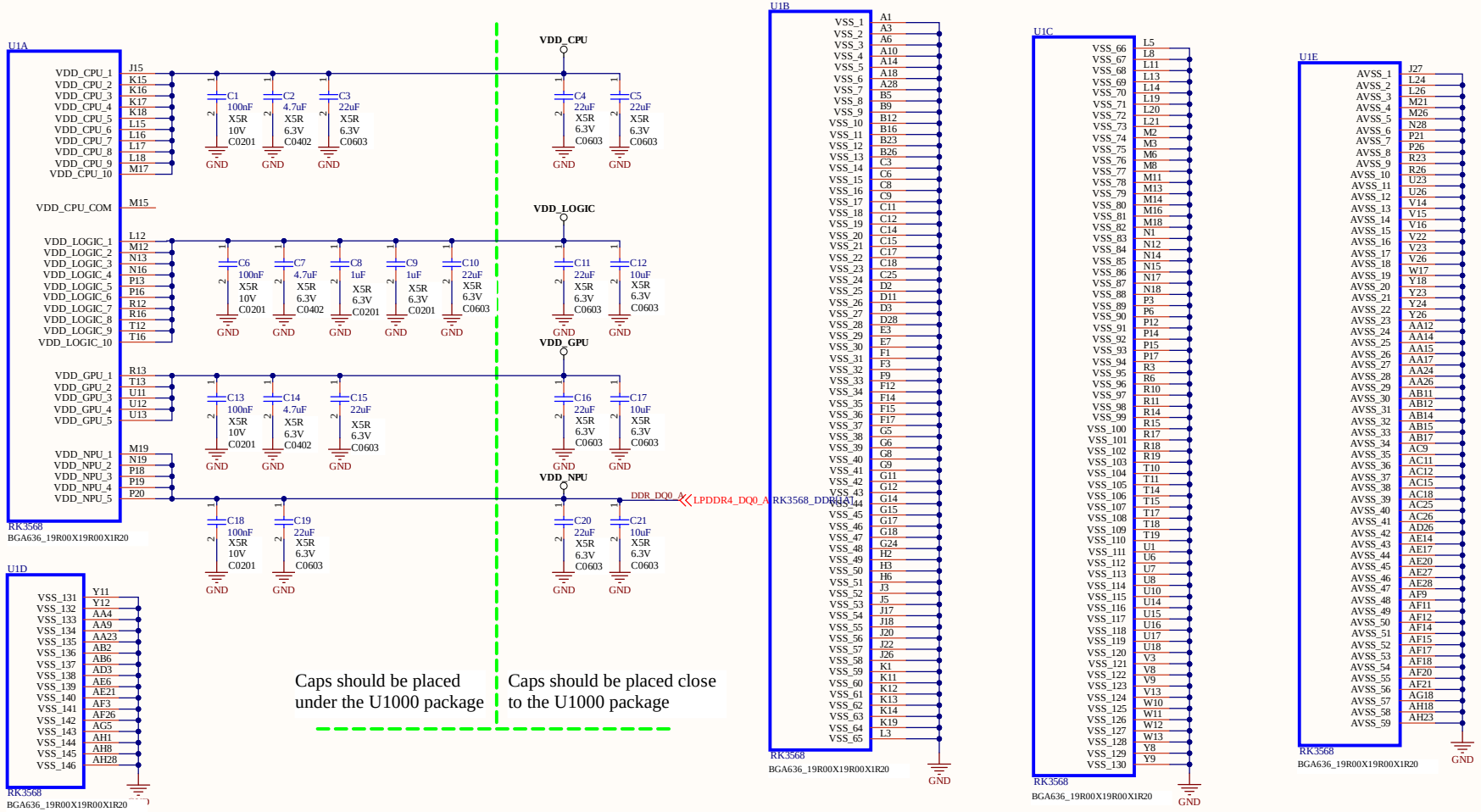
RK3568_ABCDE (Power&GND)



Size A3	Title: ROCK 3A		REV 1.3
	Page Name: RK3568_Power/GND		
Date: 9/13/2022		Sheet: 6 of 28	

RK3568_F (DDR PHY)

U1F

DDR4	LPDDR4	DDR3	LPDDR3
DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10
DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9
DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13
DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12
DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8
DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11
DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28
DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29
DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26
DDR_DQ13_A	DDR4_DQU0_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31
DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30
DDR_DQ14_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27
DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5
DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6
DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2
DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3
DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0
DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0
DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P
DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N
DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22
DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23
DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16
DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17
DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20
DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21
DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2
DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P
DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N
DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0	
DDR_ECC_DQ1	DDR4_ECC_DQ0	--	DDR3_ECC_DQ1	
DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2	
DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3	
DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4	
DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5	
DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6	
DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7	
DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM	
DDR_ECC_DQS_P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P	
DDR_ECC_DQS_N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N	

DDR4	LPDDR4	DDR3	LPDDR3	
DDR4_A0	**LPDDR4_CLKP_B**	**DDR3_A9**	---	AC0
DDR4_A1	---	DDR3_A2	---	AC1
DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6	AC2
DDR4_A3	LPDDR4_CKE1_A	DDR3_A7	---	AC3
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3	AC4
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2	AC5
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1	AC6
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---	AC7
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9	AC8
DDR4_A9	**LPDDR4_CLKN_B**	**DDR3_A5**	---	AC9
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---	AC10
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8	AC11
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---	AC12
DDR4_A13	LPDDR4_A0_A	DDR3_A14	LPDDR3_A0	AC13
DDR4_14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5	AC14
DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---	AC15
DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7	AC16
DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---	AC17
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---	AC18
DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4	AC19
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---	AC20
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---	AC21
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE	AC20
DDR4_CLKP	**LPDDR4_CLKP_A**	**DDR3_CLKP**	**LPDDR3_CLKP**	AC23
DDR4_CLKN	**LPDDR4_CLKN_A**	**DDR3_CLKN**	**LPDDR3_CLKN**	AC24
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0	AC25
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CASn	LPDDR3_ODT1	AC26
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n	AC27
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n	AC28
DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---	AC29

Note: sequences can not be swap

Note:
Except DDR3, other DQ sequences can not be swap

DDR_RZQ — H7 — R1 120R — VCC_DDR

DDR_VREFOUT — P8

DDR3L DDR3 DDR4 LPDDR3 LPDDR4 LPDDR4x	#NAME? #NAME? #NAME? #NAME? #NAME? #NAME?	DDRPHY_VDDQ1 DDRPHY_VDDQ2 DDRPHY_VDDQ3 DDRPHY_VDDQ4 DDRPHY_VDDQ5 DDRPHY_VDDQ6 DDRPHY_VDDQ7 DDRPHY_VDDQ8
DDR3L DDR3 DDR4 LPDDR3 LPDDR4 LPDDR4x	#NAME? #NAME? #NAME? #NAME? #NAME? **#NAME?**	DDRPHY_VDDQL1 DDRPHY_VDDQL2 DDRPHY_VDDQL3 DDRPHY_VDDQL4 DDRPHY_VDDQL5 DDRPHY_VDDQL6

DDR_AVSS — J8

For DDR4/DDR3/LPDDR3 mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and VSS pin

For LPDDR4/LPDDR4x mode, a 120 ohm +/-1% tolerance external resistor must be connected between the DDR_RZQ pin and DDRPHY_VDDQ

LPDDR4/LPDDR4x

VCC_DDR

C22 100nF X5R 10V C0201 — C23 100nF X5R 10V C0201 — C24 4.7uF X5R 6.3V C0402 — C25 4.7uF X5R 6.3V C0402 — C26 10uF X5R 6.3V C0603

GND

VCC_DDR

C27 100nF X5R 10V C0201 — C28 100nF X5R 10V C0201 — C29 4.7uF X5R 6.3V C0402 — C30 4.7uF X5R 6.3V C0402 — C31 4.7uF X5R 6.3V C0402

GND

Caps should be placed under the U1000 package

RK3568

BGA636_19R00X19R00X1R20

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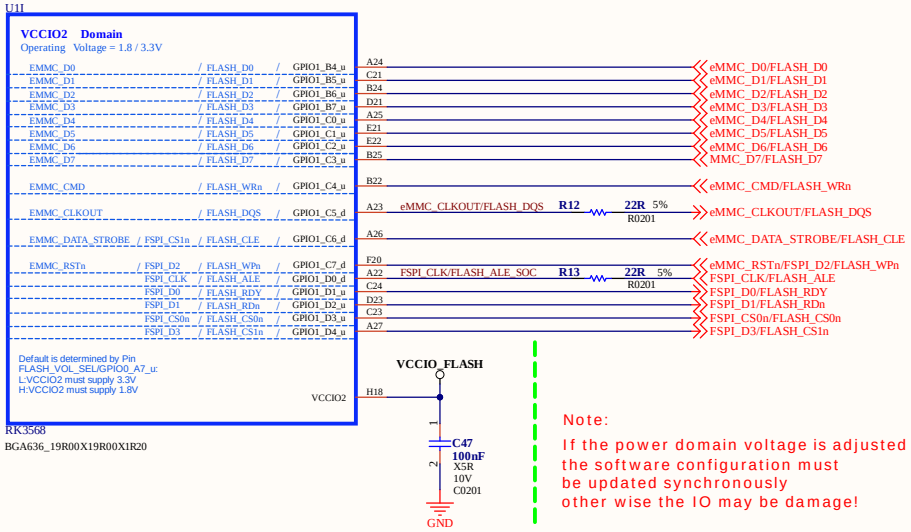
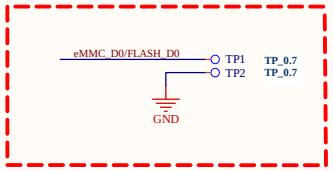
Size	Title:	REV
A3	ROCK 3A	1.3
	Page Name: RK3568_DDR PHY	
Date: 9/13/2022	Sheet: 7 of 28	

RK3568_I (VCCIO2 Domain)



Note:

If the power domain voltage is adjusted
the software configuration must
be updated synchronously
other wise the IO may be damage!

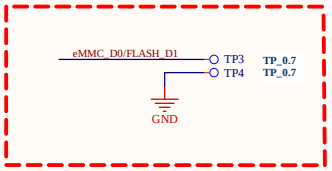


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset,
then system will enter into Maskrom mode

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

For SPI Flash:
If FSPI=0V at after power on and reset,
then system will enter into Maskrom mode

Note:

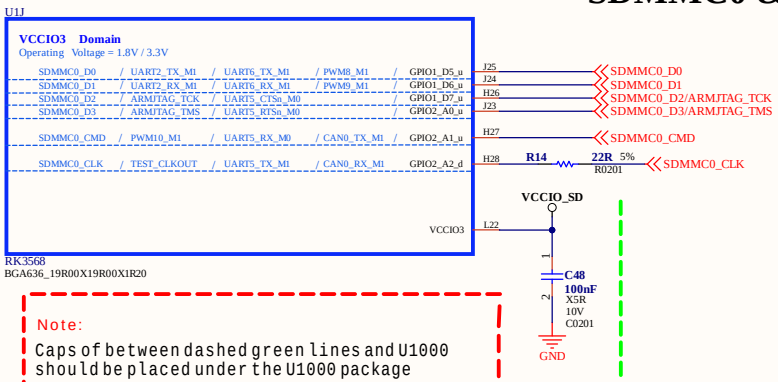
Reserve Testpoint for put the system into Maskrom mode to update the firmware when writing mismatched firmware or other conditions result in boot failure use this test point

Except in the case, please use Recovery Key
Put the system into loader mode to the firmware

RK3568_J(VCCIO3 Domain)

Default

SDMMC0 & JTAG



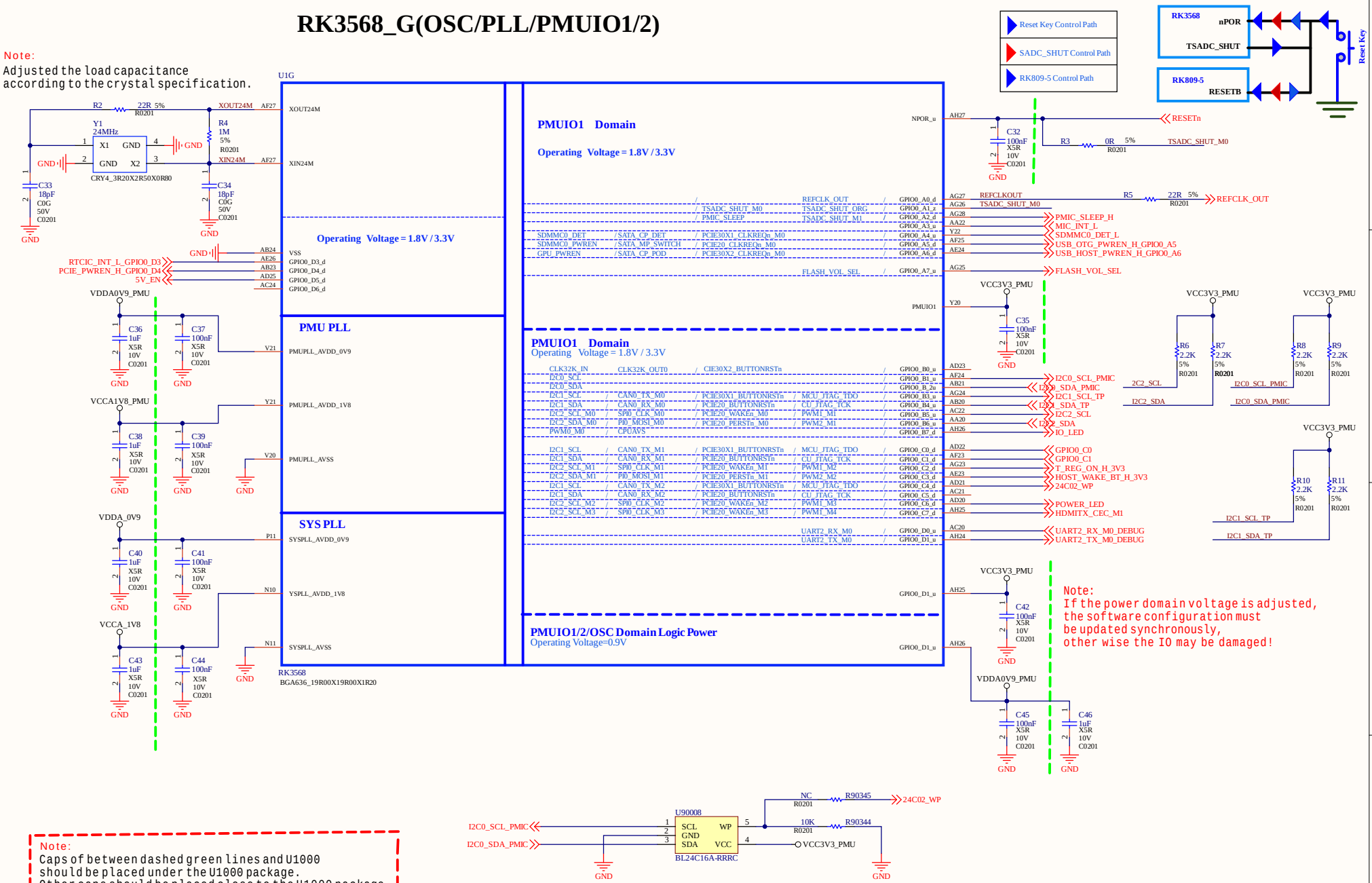
Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package

movita			
Size A3	Title: ROCK 3A		REV 1.3
	Page Name: RK3568_Flash/SD Controller		
Date: 9/13/2022		Sheet: 8 of 28	

RK3568_G(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification.

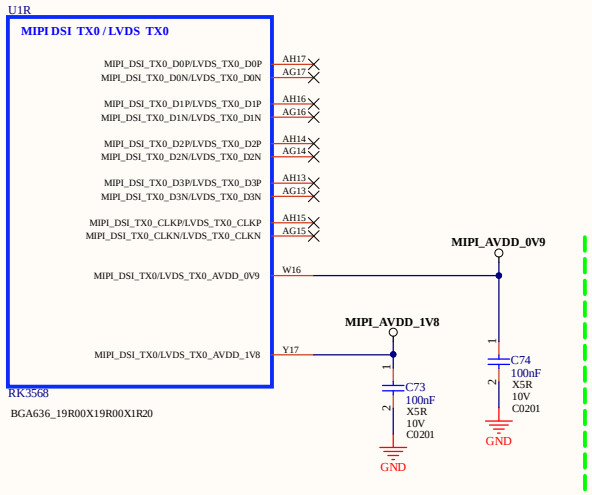


Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

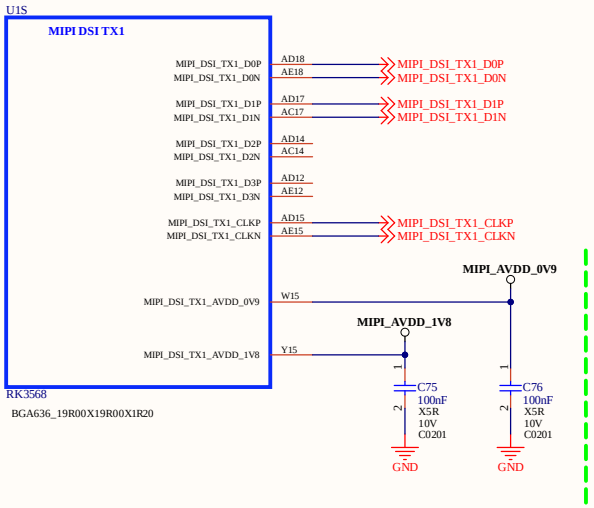
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Size A3	Title: ROCK 3A		REV 1.3
	Page Name: K3568_OSC/PLL/PMUIO		
Date: 9/13/2022		Sheet: 9 of 28	

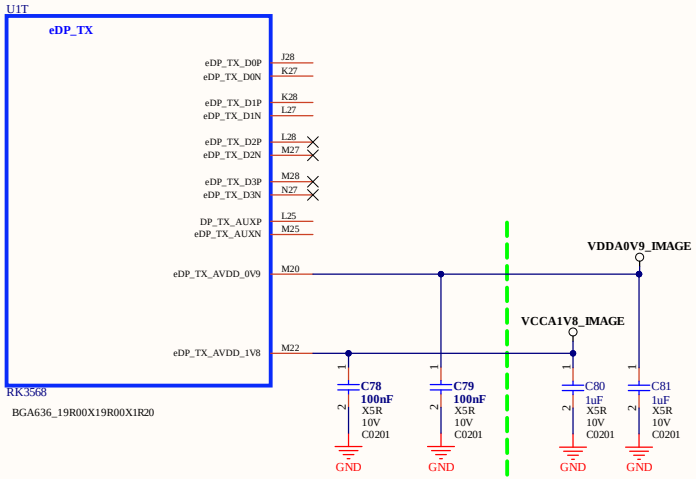
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

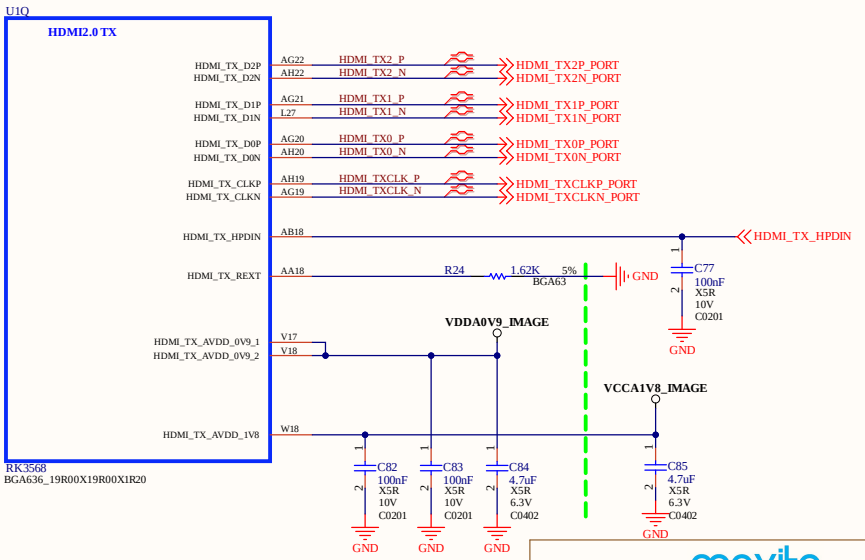


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



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Size	Title:	ROCK 3A	REV
A3	Page Name:	RK3568_VO Interface_1	1.3
Date:	9/13/2022	Sheet: 10 of 28	

RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage = 1.8V / 3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0	/	/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0	/	/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ PI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

RK3568

BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn_M1
AD7 PCIE20_WAKEn_M1
AC8 P_DET_L_GPIO2_D2
AC7
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 GPIO2_D7

AH4 GPIO3_A0

AB8
AE5 GPIO3_A2
AG4 GPIO3_A3
AF4 GPIO3_A4
AH3 GPIO3_A5
AG3 GPIO3_A6
AH2 GMAC1_INT/PMEB_GPIO3_A7
AG2 MAC1_RSTn_GPIO3_B0

AG1 PWM_FAN
AF2 GPIO3_B2
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 I2C3_SCL_M1
AE3 I2C5_SDA_M1
AD4
AC2 LCD0_PWREN_H_GPIO3_C0

AD1 PCIE20_PERSTn_M1
AD5 GPIO3_C2
AC4 GPIO3_C3

AC3 GPIO3_C4
AC2 GPIO3_C5

VCCIO5_1 V10
VCCIO5_2 V11

VCC_3V3
C86 100nF X5R 10V C0201

VCC3V3_PMU
R25 2.2K 5% R0201
GMAC1_INT/PMEB_GPIO3_A7
od

VCC_3V3
R26 2.2K 5% R0201
R27 2.2K 5% R0201
I2C5_SCL_M0
I2C5_SDA_M0

VCC_3V3
R28 2.2K 5% R0201
R29 2.2K 5% R0201
I2C3_SCL_M1
I2C3_SDA_M1

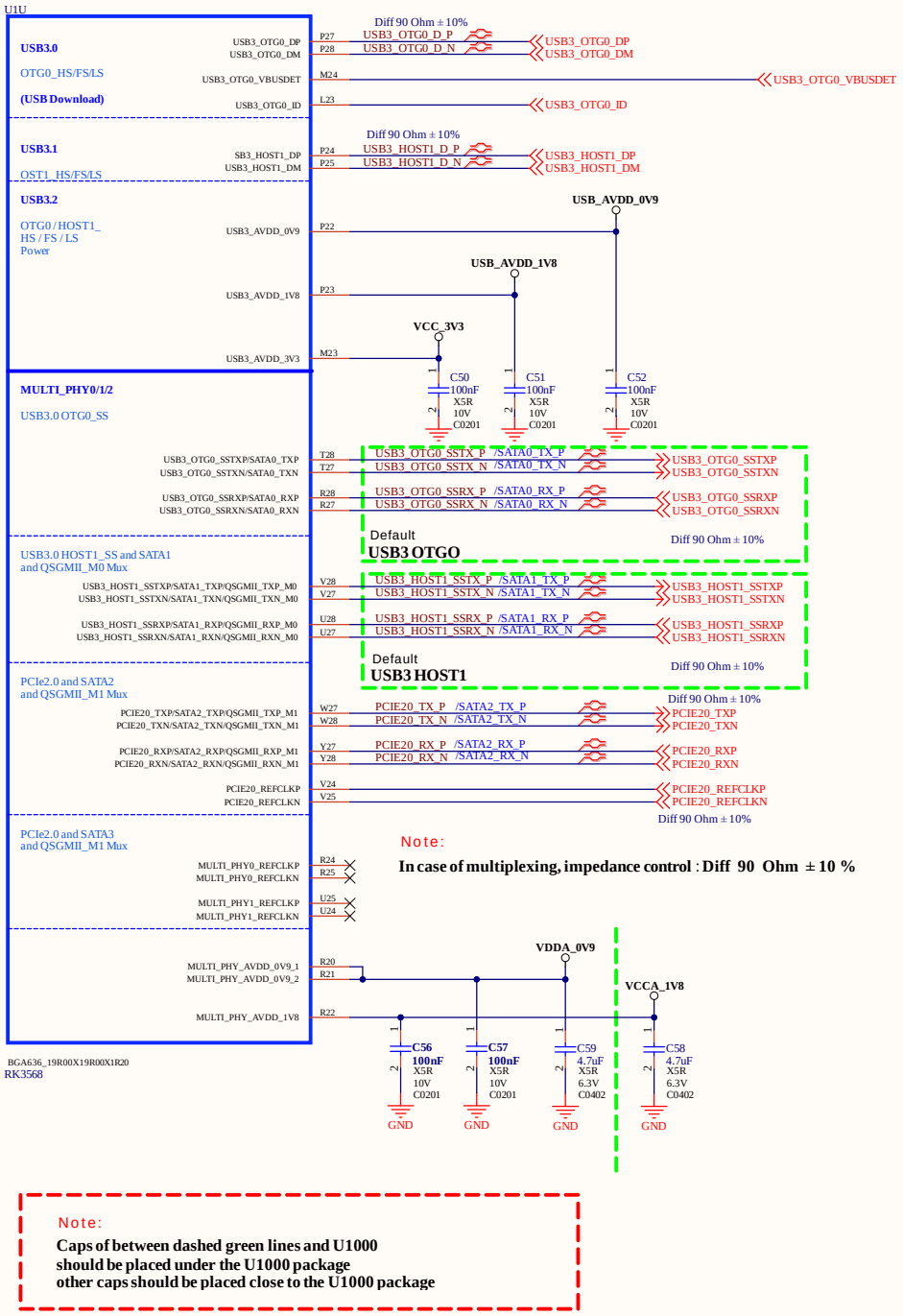
Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.

movita

Size	Title:	ROCK 3A	REV
A4	Page Name:	RK3568_VO Interface_2	1.3
Date:	9/13/2022	Sheet: 11 of 28	

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



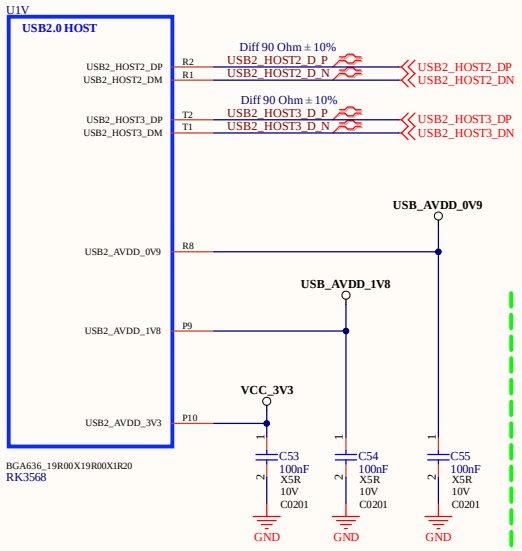
Note:

In case of multiplexing, impedance control : Diff 90 Ohm ± 10 %

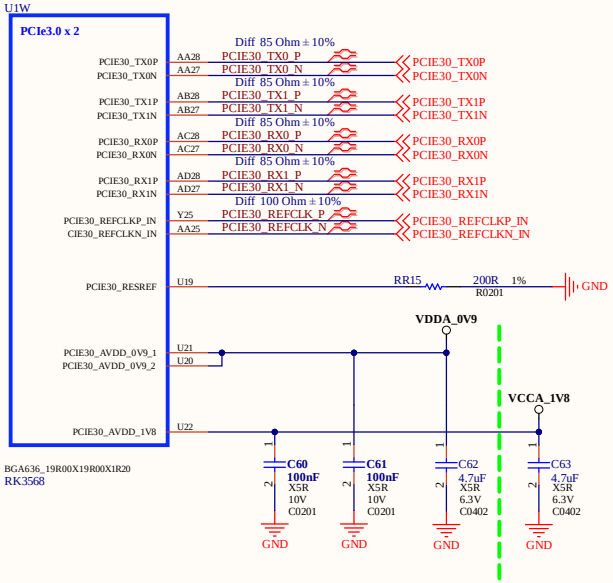
Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package
other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



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Size	Title:	ROCK 3A	REV
A3	Page Name:	Flash Power Manage	1.3
Date:	9/13/2022	Sheet: 12 of 28	

RK3568_H(VCCIO1 Domain)

U1H

VCCIO1 Domain
Operating Voltage = 1.8V / 3.3V

I2C3_SDA_M0	UART3_RX_M0	CAN1_RX_M0	AUDIOPWM_LOUT_P	ACODEC_ADC_DATA	GPIO1_A0_u	D18
I2C3_SCL_M0	UART3_TX_M0	CAN1_TX_M0	AUDIOPWM_LOUT_N	ACODEC_ADC_CLK	GPIO1_A1_u	E18
I2S1_MCLK_M0	UART3_RTSn_M0	SCR_CLK	PCIE30X1_PERSTn_M2		GPIO1_A2_d	A19
I2S1_SCLK_TX_M0	UART3_CTSn_M0	SCR_IO	PCIE30X1_WAKEn_M2	CODEC_DAC_CLK	GPIO2_A3_d	B19
I2S1_SCLK_RX_M0	UART4_RX_M0	PDM_CLK1_M0	SPDIF_TX_M0		GPIO2_A4_d	F18
I2S1_LRCK_TX_M0	UART4_RTSn_M0	SCR_RST	PCIE30X1_CLKREQn_M2	CODEC_DAC_SYNC	GPIO2_A5_d	A20
I2S1_LRCK_RX_M0	UART4_TX_M0	PDM_CLK0_M0	AUDIOPWM_ROUT_P		GPIO2_A6_d	C20
I2S1_SDO0_M0	UART4_CTSn_M0	SCR_DET	AUDIOPWM_ROUT_N	ACODEC_DAC_DATAL	GPIO2_A7_d	B20
I2S1_SDO1_M0	I2S1_SDI3_M0	PDM_SDI3_M0	PCIE20_CLKREQn_M2	ACODEC_DAC_DATAR	GPIO2_B0_d	D20
I2S1_SDO2_M0	I2S1_SDI2_M0	PDM_SDI2_M0	PCIE20_WAKEn_M2	ACODEC_ADC_SYNC	GPIO2_B1_d	E20
I2S1_SDO3_M0	I2S1_SDI1_M0	PDM_SDI1_M0	PCIE20_PERSTn_M2		GPIO2_B2_d	A21
	I2S1_SDI0_M0	PDM_SDI0_M0			GPIO2_B3_d	B21

VCCIO1 H17

RK3568
BGA636_19R00X19R00X1R20

D18 GPIO1_A0
E18 GPIO1_A1
A19 I2S1_MCLK_M0_RK809
B19 I2S1_SCLK_TX_M0_RK809
A20 I2S1_LRCK_TX_M0_RK809
C20 PDM_CLK0_M0_RK809
B20 I2S1_SDO0_M0_RK809
E20 MIPI_CAM0_PDN_L_GPIO1_B1
B21 I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCC_3V3
C87
100nF
X5R
10V
C0201
GND

Default 3.3V

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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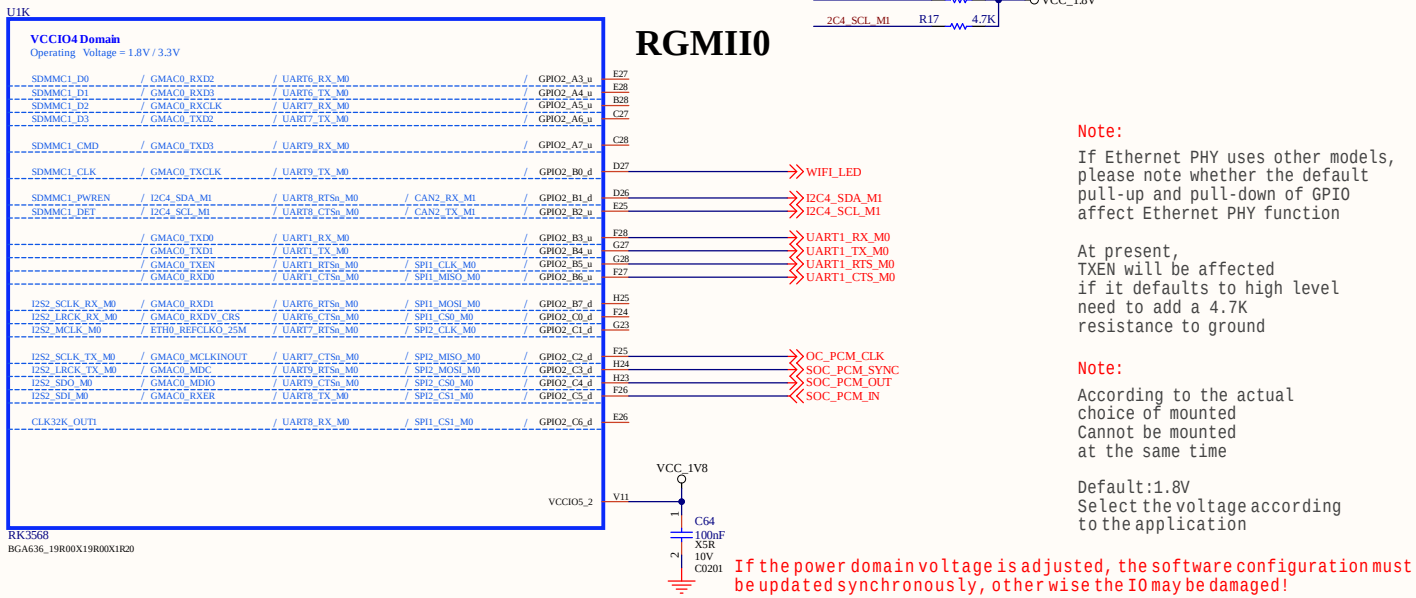
Size	Title:	ROCK 3A	REV
A4	Page Name:	RK3568_Audio Interface	1.3
Date:	9/13/2022	Sheet: 13 of 28	

RK3568_K(VCCIO4 Domain)



RGMII0

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:

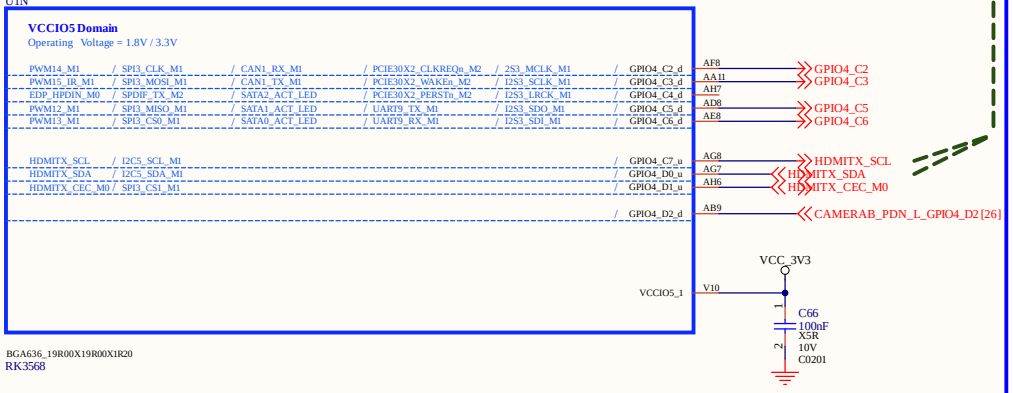
According to the actual choice of mounted Cannot be mounted at the same time

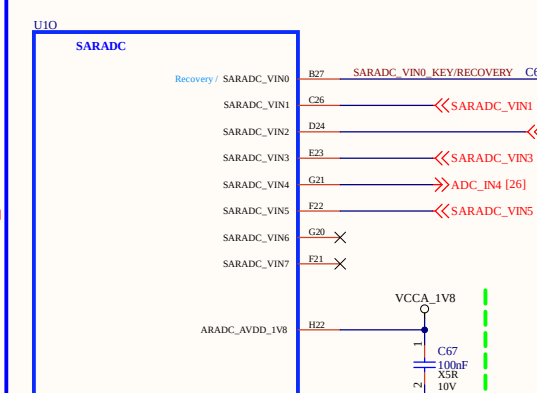
Default:1.8V
Select the voltage according to the application

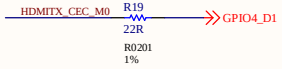
If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!

RK3568_N(VCCIO7 Domain)

Note:
When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices





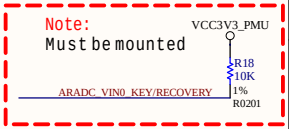


Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

RK3568_O(SARADC/OTP)

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.

Note:
Must be mounted



Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY

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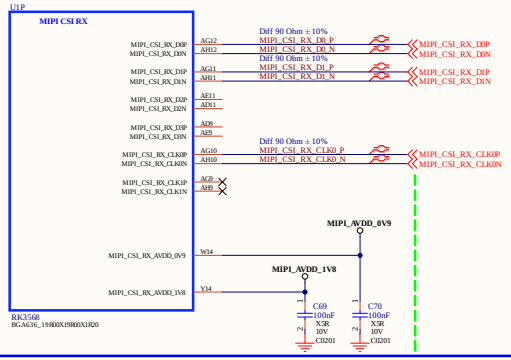
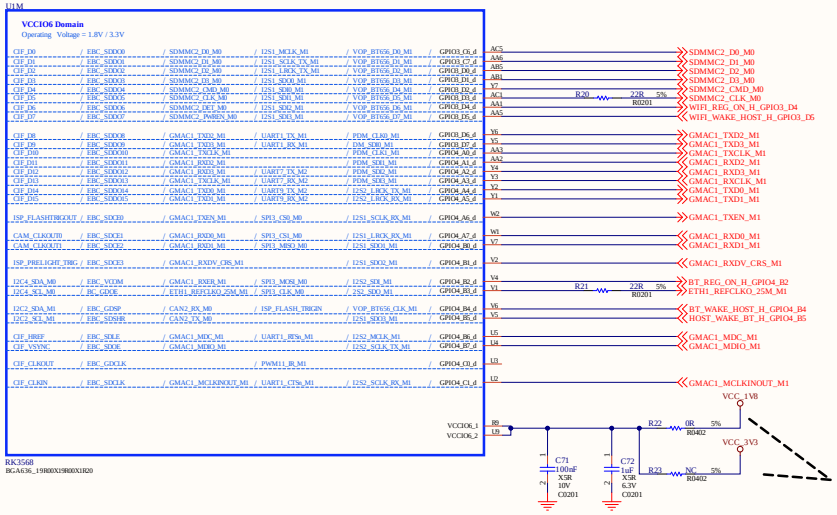
Size	Title:	ROCK 3A	REV
A3	Page Name:	K3568_SARADC/GPIO	1.3
Date:	9/13/2022	Sheet: 14 of 28	

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option1	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 IPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package other caps should be placed close to the U1000 package

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	--
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	HYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER	<-------		GMACx_RXER	<-------	
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN			
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT12(Option)	GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

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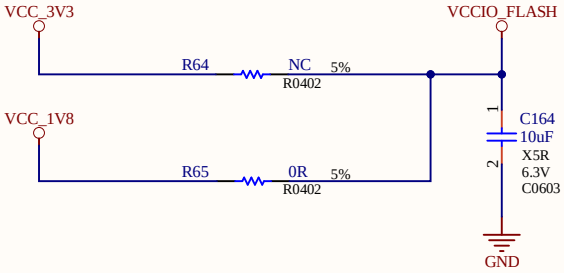
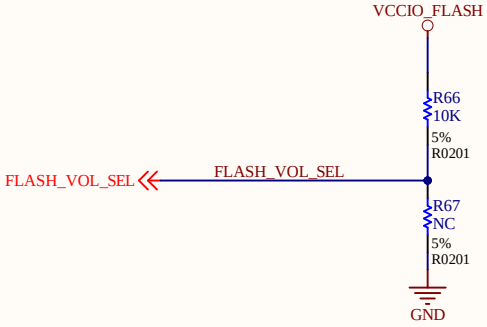
Size	Title:	REV
A2	ROCK 3A	1.3
Page Name:	RK3568_V1 Interface	
Date: 9/13/2022	Sheet: 15 of 28	

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:
According to the actual choice of mounted
Cannot be mounted at the same time





Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L : 3.3V IO driven
Logic=H : 1.8V IO driven

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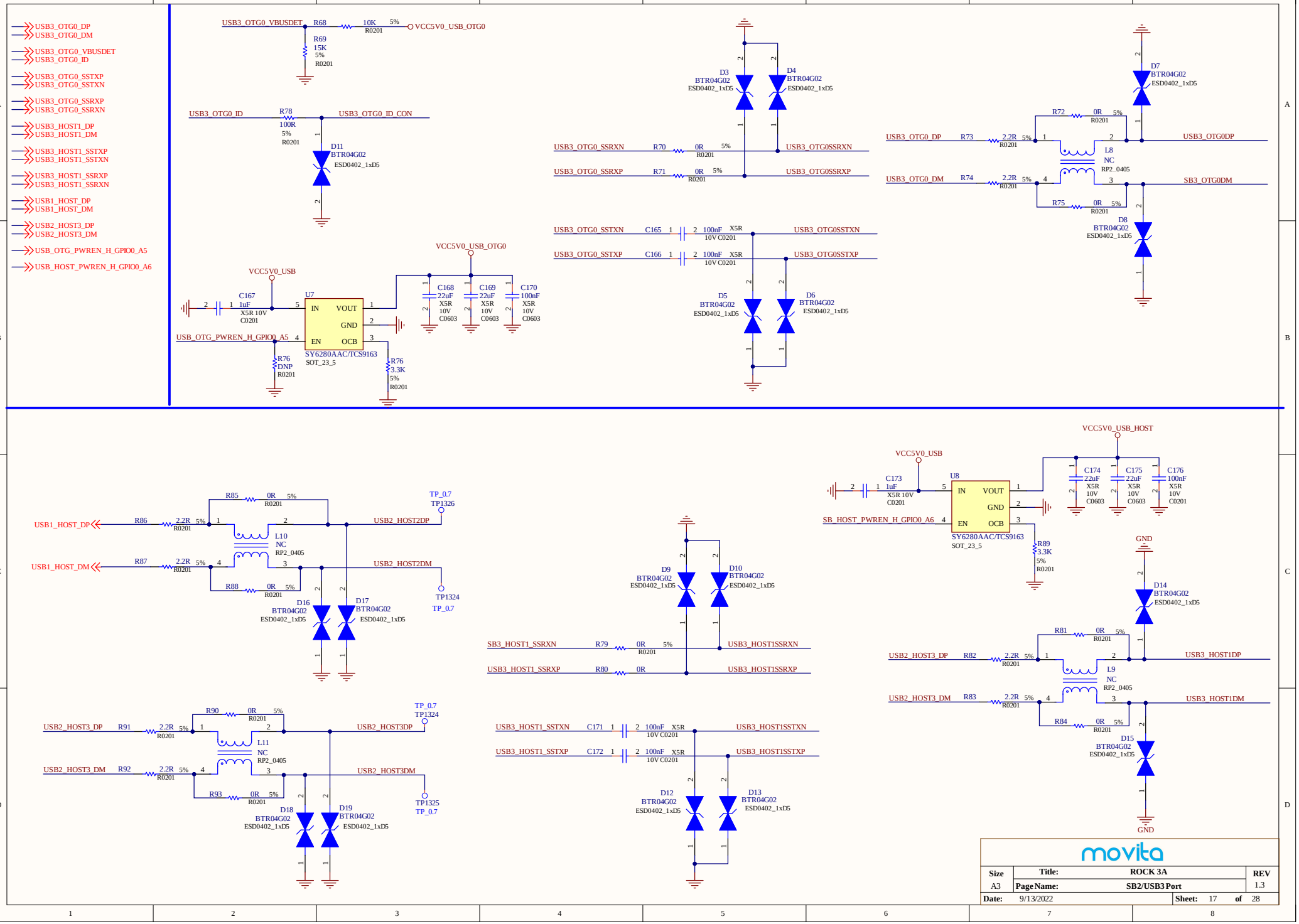
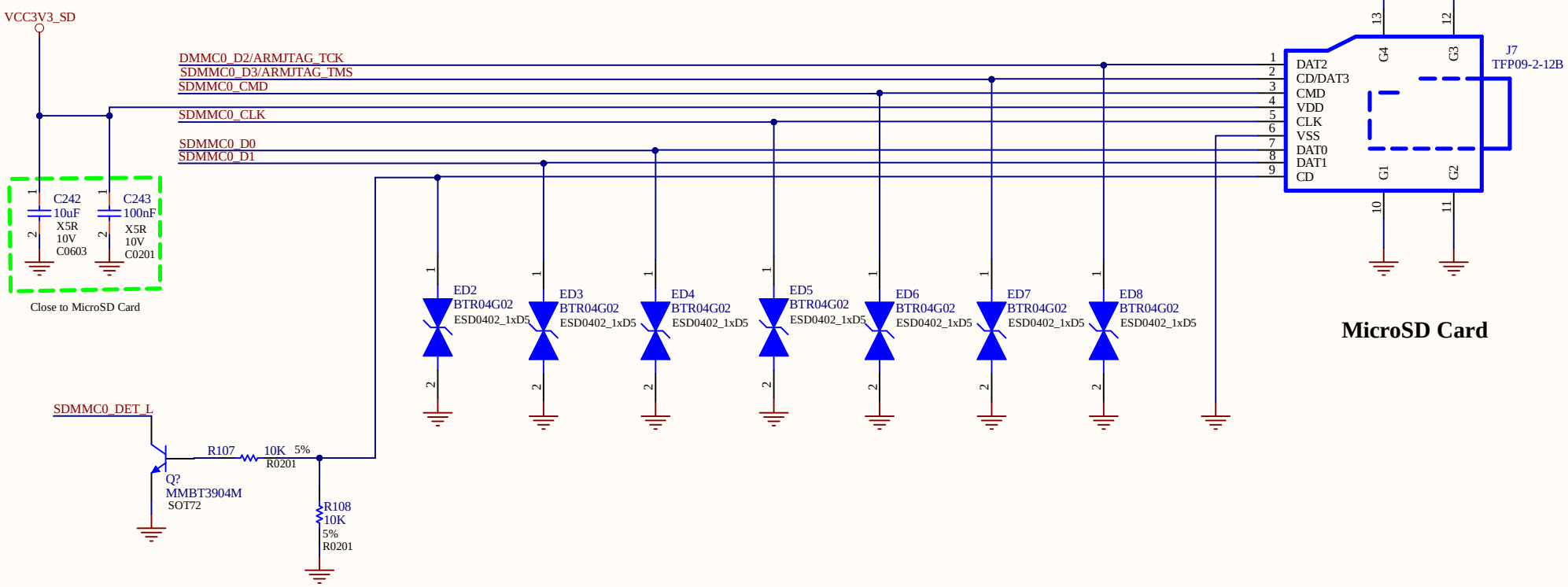
Size	Title:	ROCK 3A	REV
A4	Page Name:	Flash Power Manage	1.3
Date:	9/13/2022	Sheet: 16 of 28	


USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_ID
USB3_OTG0_SSTXP
USB3_OTG0_SSTXN
USB3_OTG0_SSRXP
USB3_OTG0_SSRXN
USB3_HOST1_DP
USB3_HOST1_DM
USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN
USB1_HOST_DP
USB1_HOST_DM
USB2_HOST3_DP
USB2_HOST3_DM
USB_OTG_PWREN_H_GPIO0_A5
USB_HOST_PWREN_H_GPIO0_A6
USB3_OTG0_VBUSDET
R68
10K
5%
R0201
VCC5V0_USB_OTG0
R69
15K
5%
R0201
USB3_OTG0_ID
R78
100R
5%
R0201
USB3_OTG0_ID_CON
D11
BTR04G02
ESD0402_1xD5
VCC5V0_USB_OTG0
VCC5V0_USB
C167
1uF
X5R 10V
C0201
U7
IN
VOUT
GND
EN
OCB
SY6280AAC/TCS9163
SOT_23_5
C168
22uF
X5R
10V
C0603
C169
22uF
X5R
10V
C0603
C170
100nF
X5R
10V
C0603
USB_OTG_PWREN_H_GPIO0_A5
R76
DNP
R0201
R76
3.3K
5%
R0201
D3
BTR04G02
ESD0402_1xD5
D4
BTR04G02
ESD0402_1xD5
USB3_OTG0_SSRXN
R70
0R
5%
R0201
USB3_OTG0SSRXN
USB3_OTG0_SSRXP
R71
0R
5%
R0201
USB3_OTG0SSRXP
USB3_OTG0_SSTXN
C165
100nF
X5R
10V C0201
USB3_OTG0SSTXN
USB3_OTG0_SSTXP
C166
100nF
X5R
10V C0201
USB3_OTG0SSTXP
D5
BTR04G02
ESD0402_1xD5
D6
BTR04G02
ESD0402_1xD5
D7
BTR04G02
ESD0402_1xD5
USB3_OTG0_DP
R73
2.2R
5%
R0201
R72
0R
5%
R0201
USB3_OTG0DP
L8
NC
RP2_0405
USB3_OTG0_DM
R74
2.2R
5%
R0201
R75
0R
5%
R0201
SB3_OTG0DM
D8
BTR04G02
ESD0402_1xD5
USB1_HOST_DP
R86
2.2R
5%
R0201
R85
0R
5%
R0201
TP_0.7
TP1326
USB2_HOST2DP
L10
NC
RP2_0405
USB1_HOST_DM
R87
2.2R
5%
R0201
R88
0R
5%
R0201
USB2_HOST2DM
TP1324
TP_0.7
D16
BTR04G02
ESD0402_1xD5
D17
BTR04G02
ESD0402_1xD5
USB2_HOST3_DP
R91
2.2R
5%
R0201
R90
0R
5%
R0201
TP_0.7
TP1324
USB2_HOST3DP
L11
NC
RP2_0405
USB2_HOST3_DM
R92
2.2R
5%
R0201
R93
0R
5%
R0201
USB2_HOST3DM
TP1325
TP_0.7
D18
BTR04G02
ESD0402_1xD5
D19
BTR04G02
ESD0402_1xD5
D9
BTR04G02
ESD0402_1xD5
D10
BTR04G02
ESD0402_1xD5
SB3_HOST1_SSRXN
R79
0R
5%
R0201
USB3_HOST1SSRXN
USB3_HOST1_SSRXP
R80
0R
USB3_HOST1SSRXP
USB3_HOST1_SSTXN
C171
100nF
X5R
10V C0201
USB3_HOST1SSTXN
USB3_HOST1_SSTXP
C172
100nF
X5R
10V C0201
USB3_HOST1SSTXP
D12
BTR04G02
ESD0402_1xD5
D13
BTR04G02
ESD0402_1xD5
VCC5V0_USB_HOST
VCC5V0_USB
C173
1uF
X5R 10V
C0201
U8
IN
VOUT
GND
EN
OCB
SY6280AAC/TCS9163
SOT_23_5
C174
22uF
X5R
10V
C0603
C175
22uF
X5R
10V
C0603
C176
100nF
X5R
10V
C0201
SB_HOST_PWREN_H_GPIO0_A6
R89
3.3K
5%
R0201
GND
D14
BTR04G02
ESD0402_1xD5
USB2_HOST3_DP
R82
2.2R
5%
R0201
R81
0R
5%
R0201
USB3_HOST1DP
L9
NC
RP2_0405
USB2_HOST3_DM
R83
2.2R
5%
R0201
R84
0R
5%
R0201
USB3_HOST1DM
D15
BTR04G02
ESD0402_1xD5
GND
movita
Size
A3
Title:
ROCK 3A
REV
1.3
Page Name:
SB2/USB3 Port
Date:
9/13/2022
Sheet:
17
of
28

MicroSD Card

SDMMC0_D0
SDMMC0_D1
SDMMC0_D2/ARMJTAG_TCK
SDMMC0_D3/ARMJTAG_TMS
SDMMC0_CMD
SDMMC0_CLK
DMMC0_DET_L



MicroSD Card

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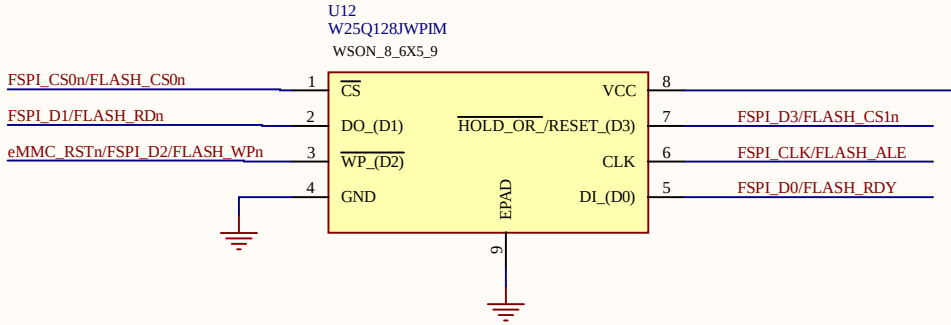
Size	Title:	ROCK 3A	REV
A4	Page Name:	MicroSD Card	1.3
Date:	9/13/2022	Sheet: 18 of 28	

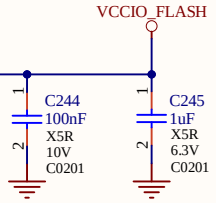
SPI Flash

FSPI_CLK/FLASH_ALE

FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

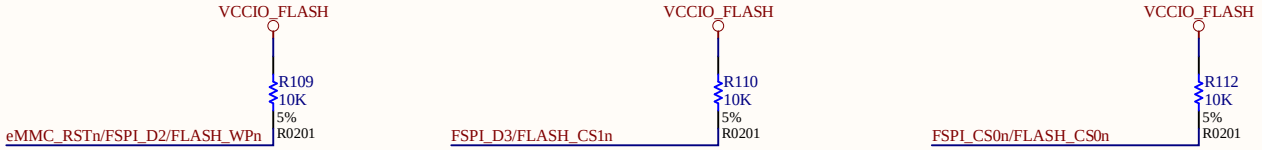
FSPI_CS0n/FLASH_CS0n





Note:
Default: 1.8V

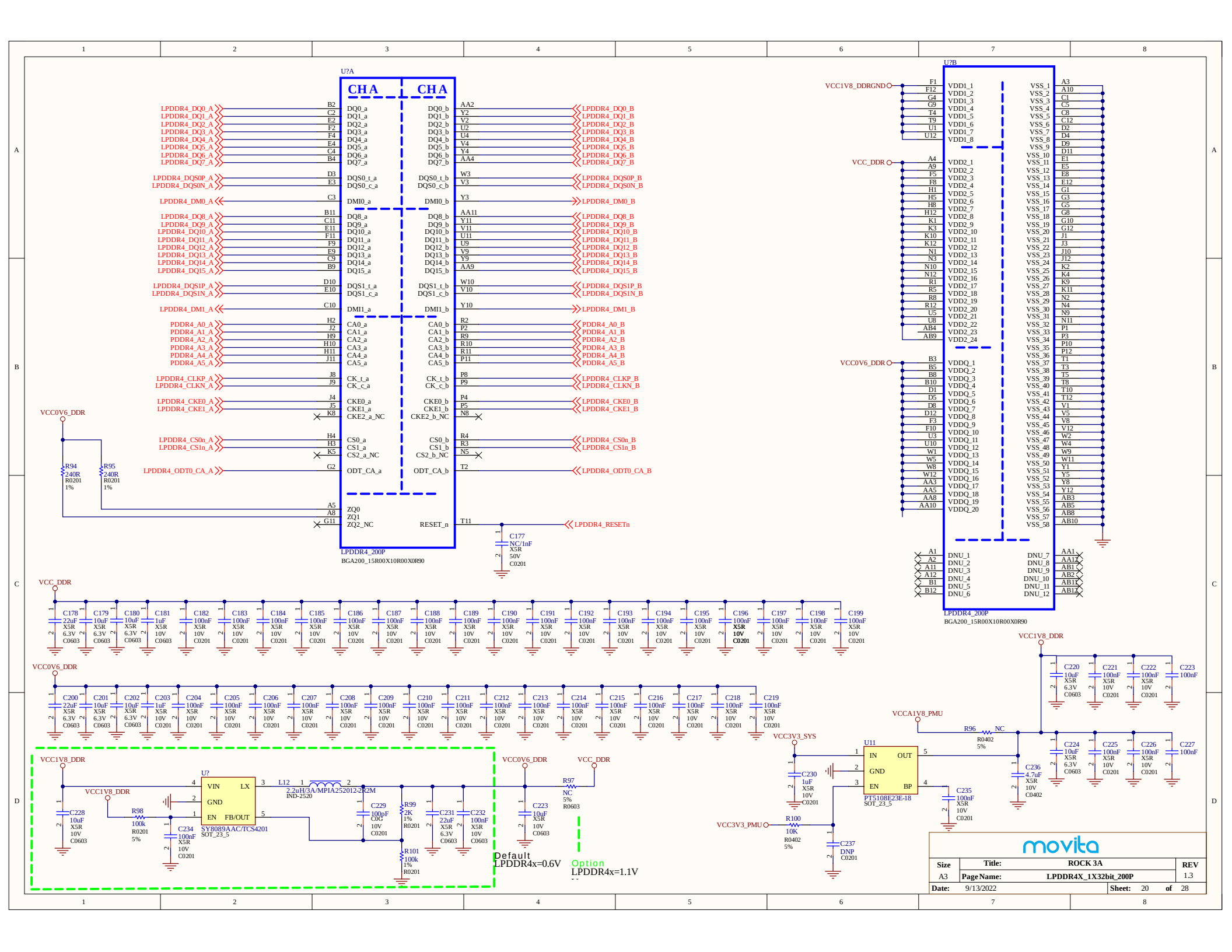
Support:
1bit SPI NOR or SPI NAND
4bit SPI NOR or SPI NAND



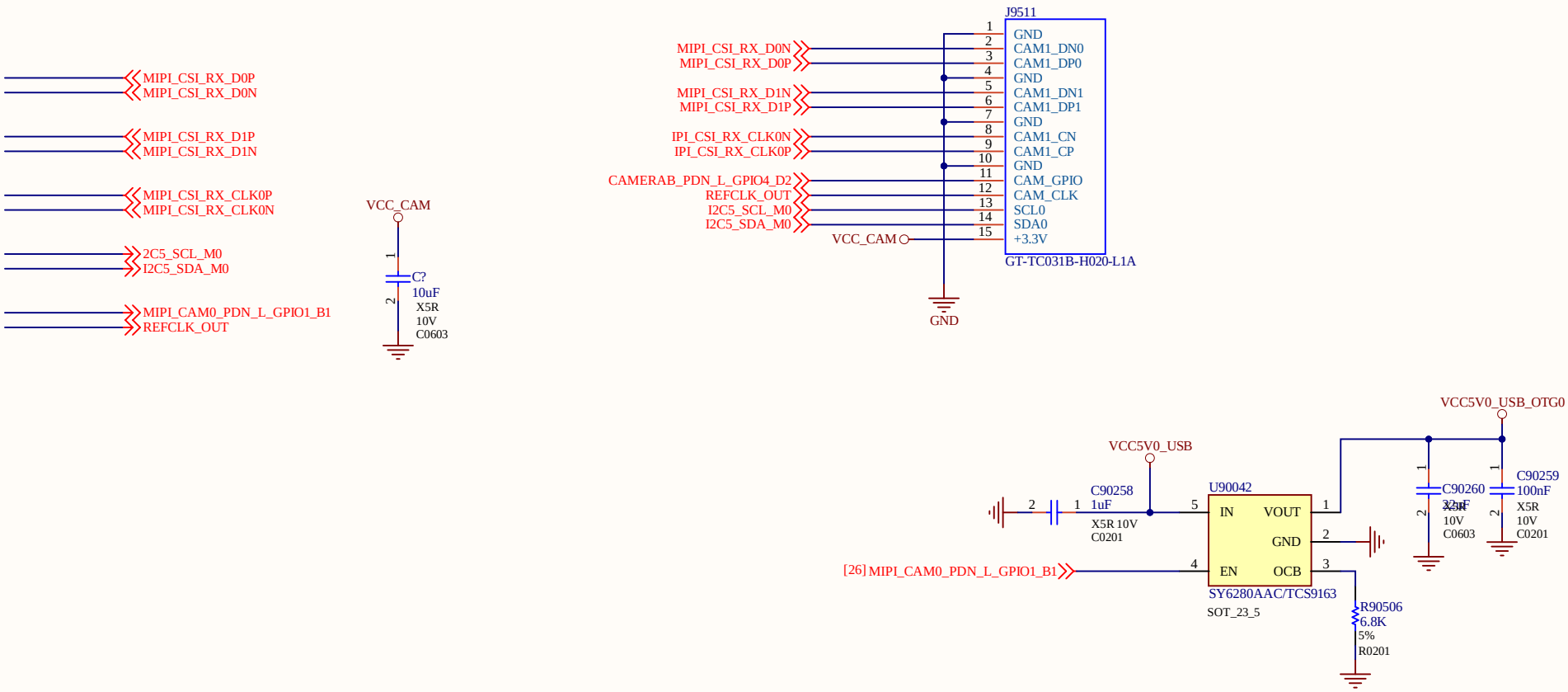
Note:
If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

movita

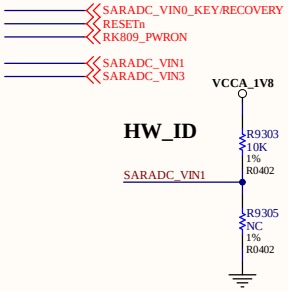
Size	Title:	ROCK 3A	REV
A4	Page Name:	SPI FLASH(Option)	1.3
Date:	9/13/2022	Sheet: 19 of 28	


U?A
CHA
CHA
LPDDR4_200P
BGA200_15R00X10R00X0R90
U?B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC0V6_DDR
VCC_DDR
VCC1V8_DDR
VCC1V8_DDRGND
VCC0V6_DDR
VCC_DDR
VCC1V8_DDR
VCC0V6_DDR
VCC1V8_DDR
VCC1V8_DDR
VCC1V8_DDR
VCC0V6_DDR
VCC_DDR
VCC3V3_SYS
VCCA1V8_PMU
VCC3V3_PMU
SY8089AAC/TCS4201
SOT_23_5
PT5108E23E-18
SOT_23_5
Default
LPDDR4x=0.6V
Option
LPDDR4x=1.1V
movita
Size
A3
Title:
ROCK 3A
REV
1.3
Page Name:
LPDDR4X_1X32bit_200P
Date:
9/13/2022
Sheet:
20
of
28

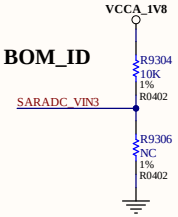
MIPI_CSI_RX 2Lanes



movita			
Size A4	**Title:** ROCK 3A		**REV** 1.3
	Page Name: MIPI_DSI_CSI		
Date: 9/13/2022		**Sheet:** 21 **of** 28	

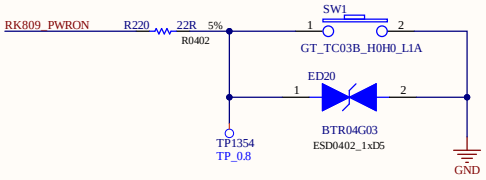


SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

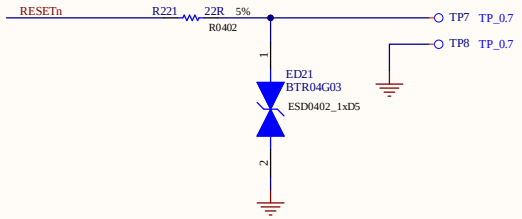


SARADC_VIN1	Up Resistance	Down Resistance
HW_ID1	10K	DNP
HW_ID2	10K	110K
HW_ID3	20K	100K
HW_ID4	33K	100K
HW_ID5	18K	36K
HW_ID6	36K	51K
HW_ID7	51K	51K
HW_ID8	51K	36K
HW_ID9	36K	18K
HW_ID10	100K	33K
HW_ID11	100K	20K
HW_ID12	110K	10K
HW_ID13	DNP	10K

PowerOn/OFF_Key



Reset_Key

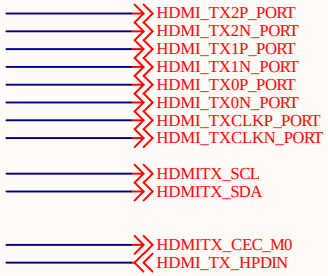


Note:

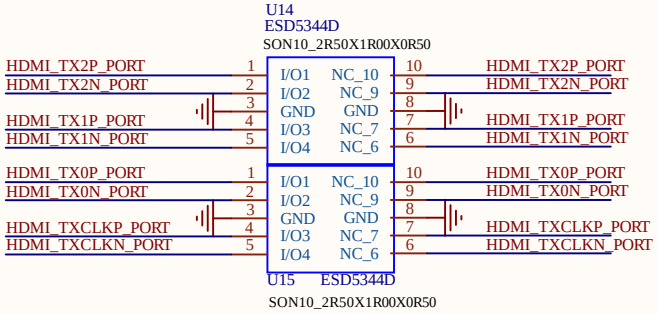
If there is no Key requirement, It is suggested to reserve a SW9200 Key to facilitate the development debug

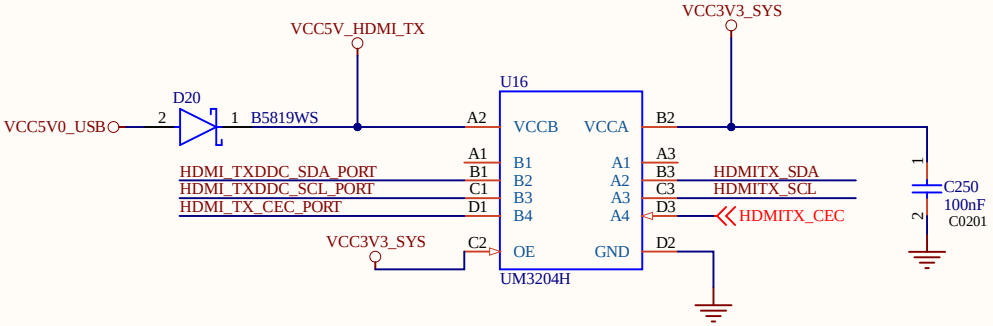
Size: A3	Title: ROCK 3A	REV: 1.3
	Page Name: SARADC_KEY	
Date: 9/13/2022	Sheet: 22 of 28	

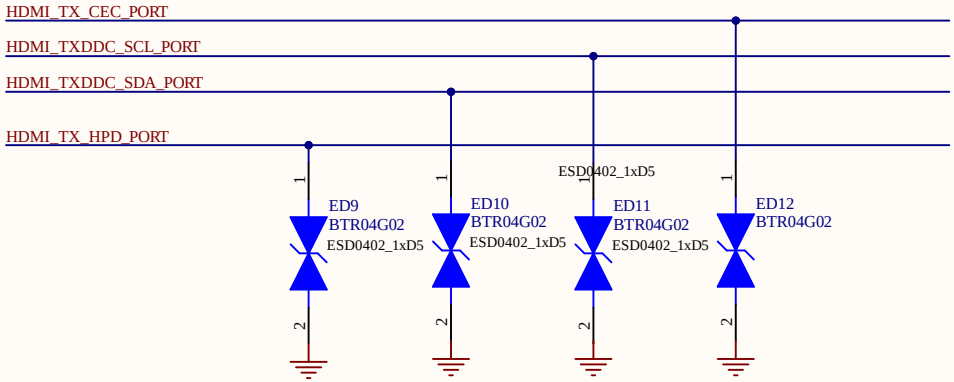
HDMI2.0 TX

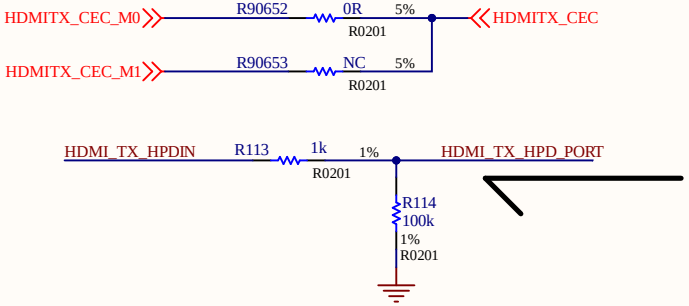


Cj<=0.4pF







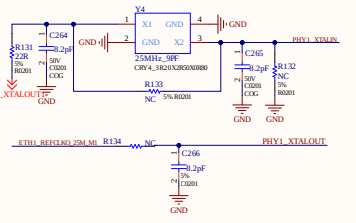


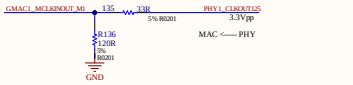
movita

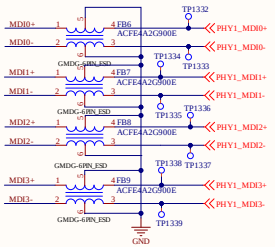
Size	Title:	ROCK 3A	REV
A4	Page Name:	HDMI	1.3
Date:	9/13/2022	Sheet: 23 of 28	

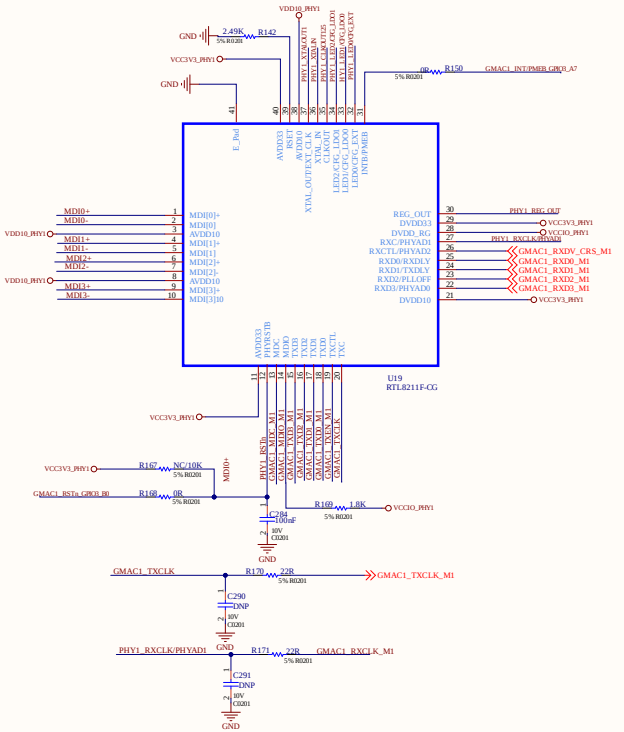
Giga PHY1

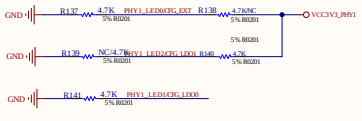
GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO3_B0
GMAC1_INT/PMEB_GPIO3_A7

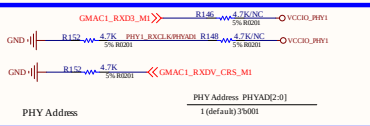


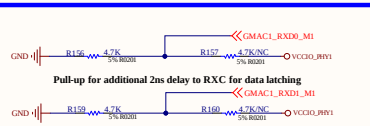


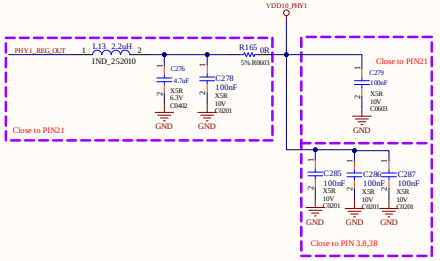




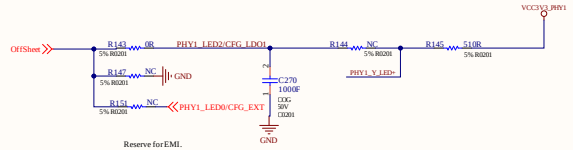


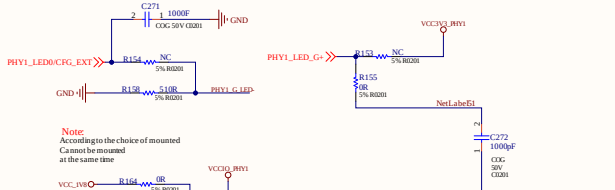


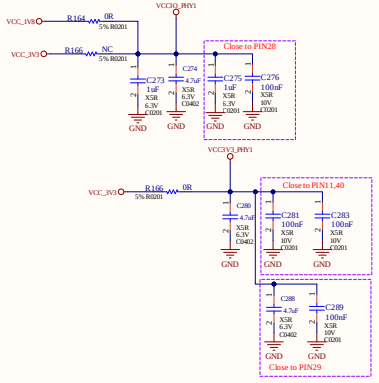




RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	

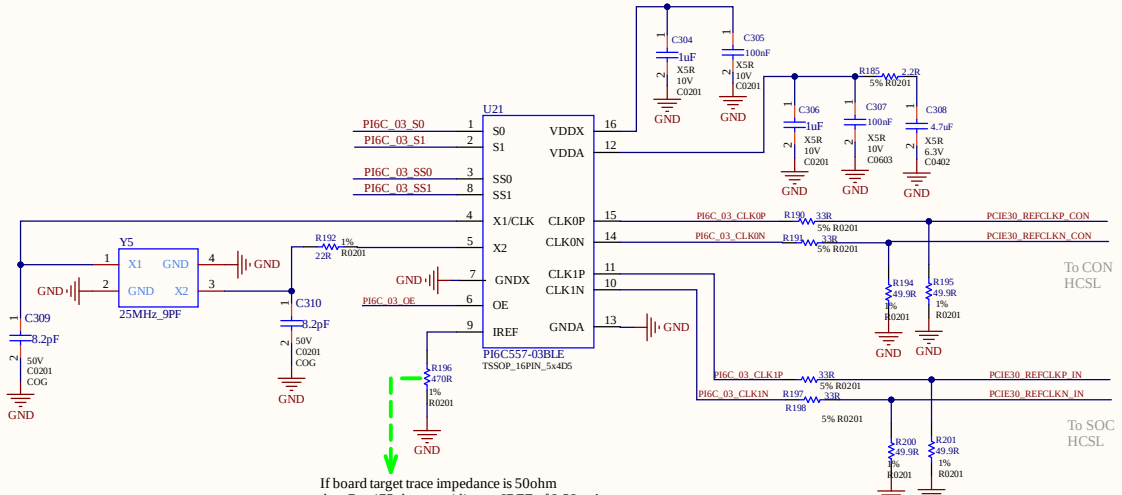






movita

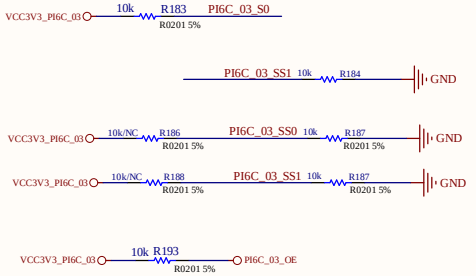
Size	Title:	REV
A2	ROCK 3A	1.3
	Page Name: Ethernet	
Date: 9/13/2022	Sheet: 24 of 28	

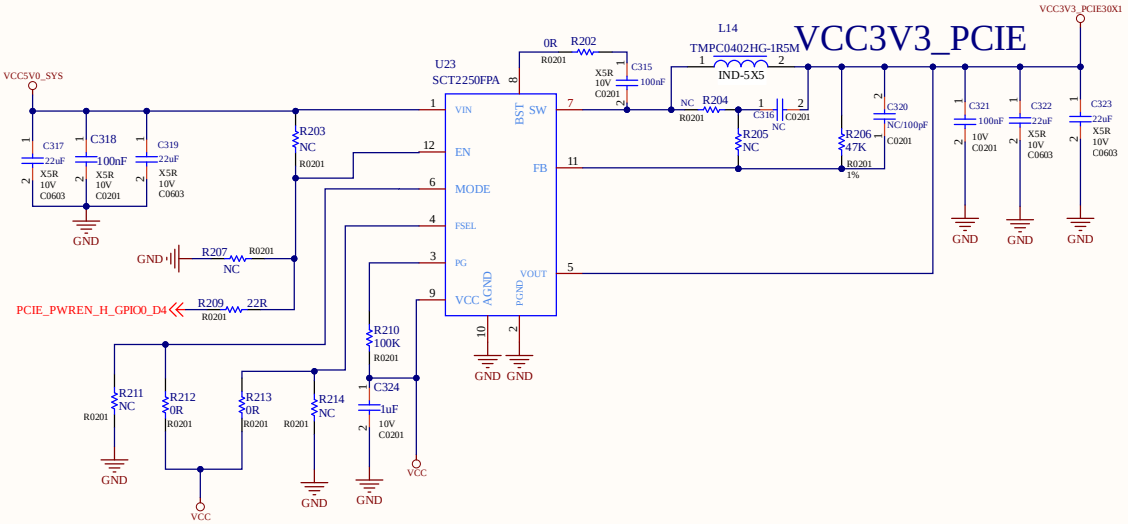


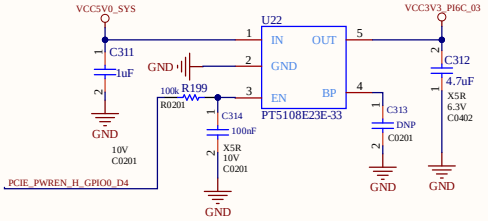
If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA .
The output current (IOH) is 6 * IREF .
6x2.32X50=696mV

PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread







movita

Size	Title:	REV
A3	Page Name: ROCK 3A MKEY_PCIE3.0	1.3
Date: 9/13/2022	Sheet: 25 of 28	

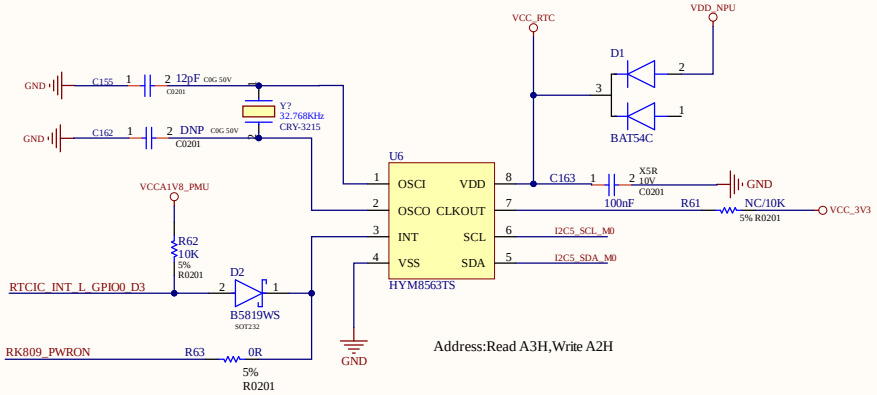
I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_COM
RTCIC_INT_L_GPIO0_D3
RTCIC_32KOUT
I2C5_SCL_M0
I2C5_SDA_M0
RK809_PWRON

VDD_CPU

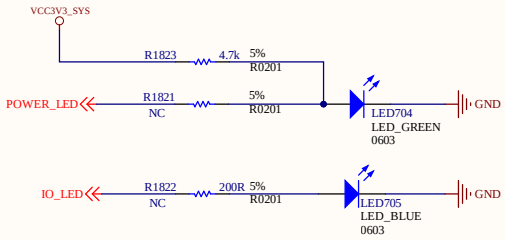
RTC IC --Option

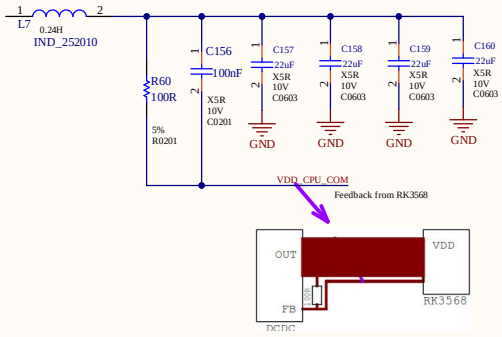
Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC
But, it will not support the timing poweron function



Address:Read A3H,Write A2H





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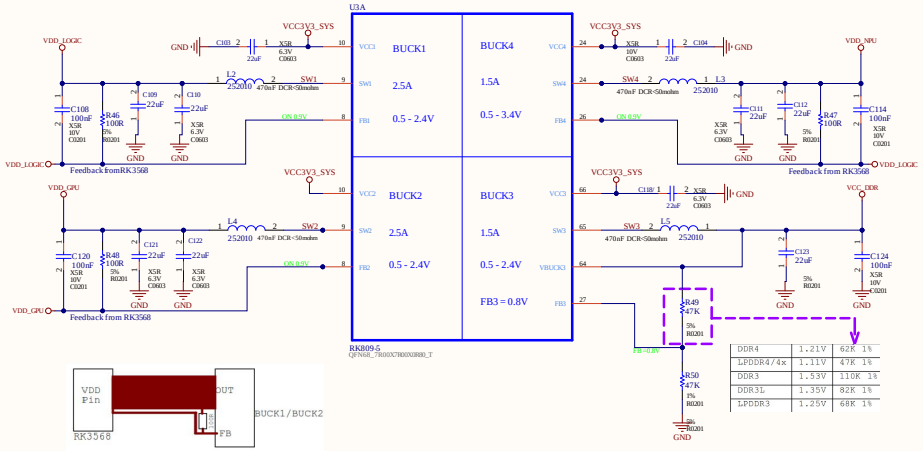
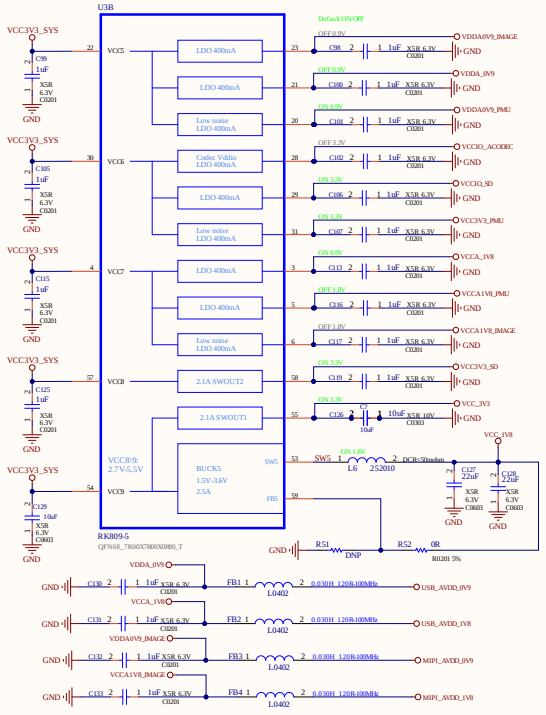
Size	Title:	ROCK 3A	REV
A3	PageName:	Power_CPU_RTC	1.3
Date:	9/13/2022	Sheet: 26 of 28	

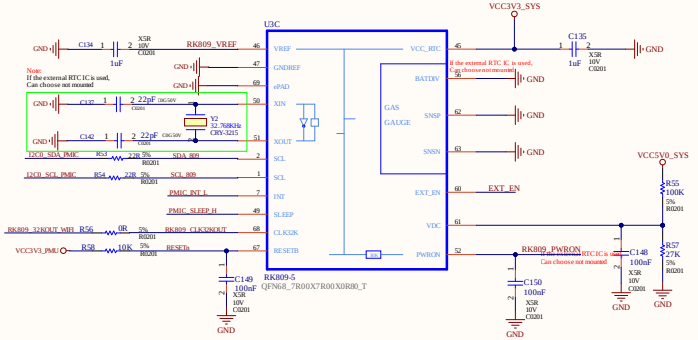
PMIC RK809 DCDC



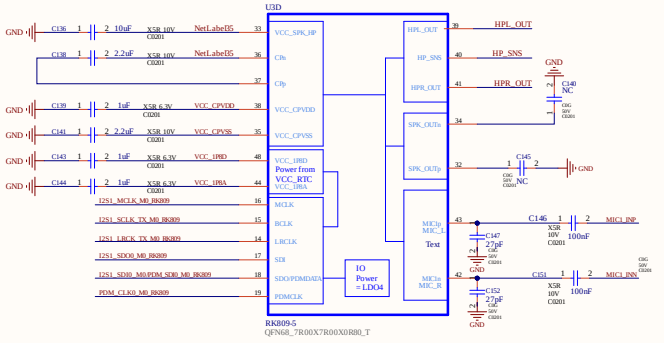
PMIC RK809 LDO



PMIC RK809 Managerment

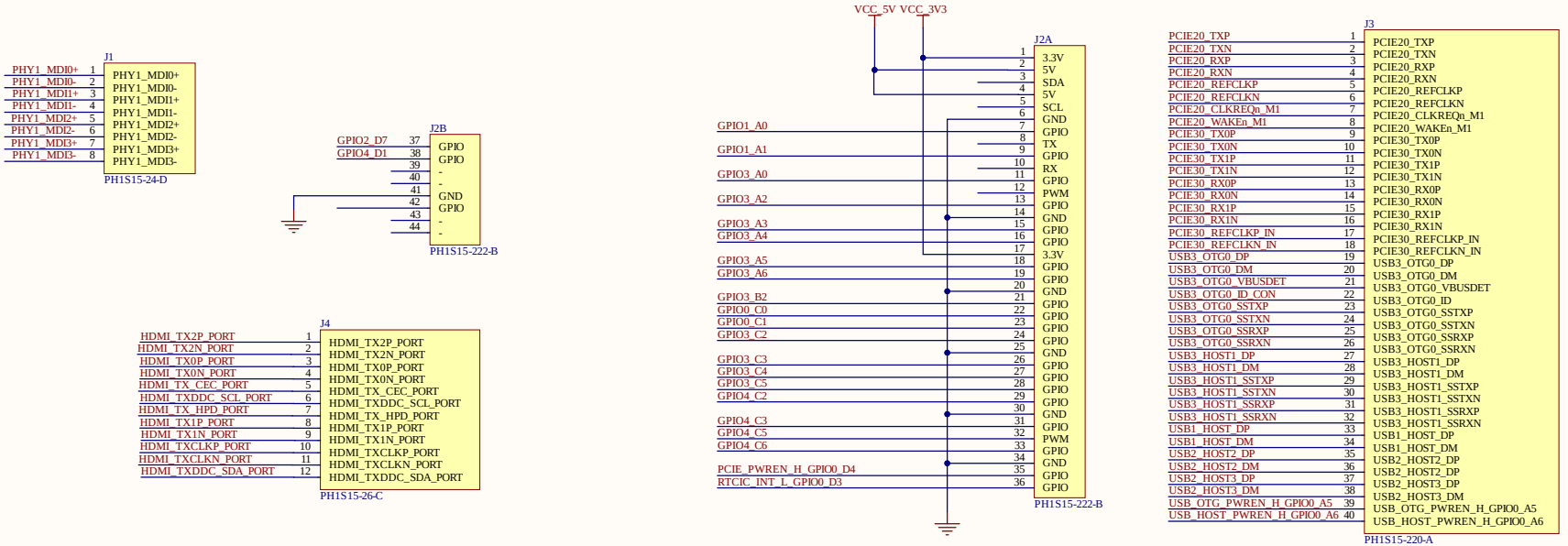


PMIC RK809 CODEC



Note:
If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

Size	Title:	ROCK 3A	REV
A2	Page Name:	Power_PMIC	1.3
Date:	9/13/2022	Sheet: 27 of 28	



movita

Size	Title:	REV
A3	ROCK 3A	1.3
	Page Name: IO_CONNECTORS	
Date: 9/13/2022	Sheet: 28 of 28	